IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/538,369
Applicant(s)	:	Geoffrey F. BURNS et al.
Filed	:	13 June 2005
TC/A.U.	:	2183
Confirmation	:	6028
Examiner	:	Vincent Fong
Atty. Docket	:	US-020543US

Title: MODULATOR INTEGRATION OF AN ARRAY PROCESSOR WITHIN A SYSTEM ON CHIP

APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop **Appeal Brief - Patents**
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Sir:

In response to the FINAL Office Action dated 23 August 2007, finally rejecting pending claims 1-8 and 11-18 and 20-23, and in support of the Notice of Appeal filed on 6 November 2007, Applicants hereby respectfully submit this Appeal Brief.

REAL PARTY IN INTEREST

According to an assignment recorded at Reel 019719, Frame 0843, NXP, B.V., owns all of the rights in the above-identified U.S. patent application.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to this application or to any related application, nor will the disposition of this case affect, or be affected by, any other application directly or indirectly.

STATUS OF CLAIMS

Claims 1-8 and 11-18 and 20-23 are pending and all stand rejected. Claims 9, 10 and 19 are canceled.

Accordingly, the claims on Appeal are claims 1-8 and 11-18 and 20-23.

STATUS OF AMENDMENTS

There are no pending amendments with respect to this application.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to coprocessor, a coprocessing system, an integrated circuit including a coprocessor, a system including a coprocessor, a functional unit having a two-dimensional array of processing cells, and a method for interfacing a coprocessor to a main processor.[1]

Accordingly, as broadly recited in claim 1, a coprocessor (FIG. 1 – 30; FIG. 2 – 106; page 4, lines 9-10; page 5, lines 13-14) to a main processor (FIG. 1 – 20) having an execution speed greater than that of the processor (page 4, lines 12-15), comprises a two-dimensional array (FIG. 2 – 108; page 4, lines 10-11) of processing cells (FIG. 2 – 112; page 5, lines 10-11) and being communicatively connected to the processor by an interface module (FIG. 1 – 40; FIG. 2 – 110; page 4, lines 17-19; page 5, lines 14-15) having a mechanism for reconfiguring a plurality of information paths (FIG. 2 – 122, 124; page 6, lines 13-26) between the interface module and respective cells on a periphery of the array (page 6, lines 1-7).

As broadly recited in claim 2, the coprocessor further features the array comprising a systolic processing array (page 6, lines 27-28).

As broadly recited in claim 3, the coprocessor further features the paths being

1 In the description to follow, citations to various reference numerals, figures, and corresponding text in the specification are provided solely to comply with Patent Office rules. It should be understood that these reference numerals, figures, and text are exemplary in nature, and not in any way limiting of the true scope of the claims. It would therefore be improper to import anything into any of the claims simply on the basis of **exemplary** language that is provided here only under the obligation to satisfy Patent Office rules for maintaining an Appeal.

connected one-to-one with the respective cells (page 6, lines 15-17).

As broadly recited in claim 5, the coprocessor further features inter-cell connection within the array such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent (page 5, lines 27-29; page 6, lines 7-8).

As broadly recited in claim 11, the processor further comprises a digital signal processor (page 4, lines 8-9).

As broadly recited in claim 13, a functional unit (FIG. 2 – 100) having two-dimensional array (FIG. 2 – 108) of processing cells (FIG. 2 – 112) and serving as a component of a main processor, has a mechanism for reconfiguring a plurality of intra-processor information paths (FIG. 2 – 122, 124) to the array to respective cells on a periphery of the array.

As broadly recited in claim 14, the unit further features the processor comprising a very long instruction word (VLIW) processor (Fig. 3; page 9, lines 7-10).

As broadly recited in claim 15, the unit further features inter-cell connection within the array such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent (page 5, lines 27-29; page 6, lines 7-8).

As broadly recited in claim 16, the unit further features means (Fig. 3 – 126; page 8, lines 16-20; page 10, lines 14-16) for transmitting a plurality of array programs to corresponding predetermined subsets of the processing cells.

As broadly recited in claim 17, a system further features an array program generator (FIG. 3 – 310; page 9, lines 13-14) for generating array programs to be transmitted, and, when needed, updating a program (FIG. 4 – 406; page 9, lines 21-24), transmitting the updated program (FIG. 4 – 412; page 10, line 30 – page 11, line 2), and transmitting concurrently, when needed, a reconfigure signal to the mechanism to correspondingly update a current steady state connection pattern of the information paths (FIG. 4 – 414, 416; page 9, lines 9-14).

As broadly recited in claim 18, the system further features a compiler (FIG. 3 –

312; page 9, line 14) configured for receiving, in response to the program updating, data representative of input and output timing for the unit and further configured for compiling an instruction based on the data (page 10, lines 26-30).

As broadly recited in claim 20, a method for interfacing a coprocessor to a main processor, comprises the steps of: configuring the coprocessor (FIG. 1 – 30; FIG. 2 – 106; page 4, lines 9-10; page 5, lines 13-14) to compromise a two-dimensional array (FIG. 1 – 108; page 4, lines 10-11) of processing cells (FIG. 1 – 112; page 5, lines 10-11) and to have an execution speed greater than that of the processor (page 4, lines 12-15); and communicatively connecting the coprocessor to the processor by an interface module (FIG. 1 – 40; FIG. 2 – 110; page 4, lines 17-19; page 5, lines 14-15) having a mechanism for reconfiguring a plurality of information paths (FIG. 2 – 122, 124; page 6, lines 13-26) between the interface module and respective cells on a periphery of the array (page 6, lines 1-7).

As broadly recited in claim 21, the array is rectangular (see FIG. 2; page 5, line 7-8), wherein the periphery consists of those of the processing cells located in all of a first row, last row, first column and last column of the array (see FIG. 2; page 6, lines 4-7), and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array (page 6, lines 13-23).

As broadly recited in claim 22, the interface comprises a plurality of border cells (114; page 6, lines 1-3) directly connected to the respective processing cells on the periphery of the array.

As broadly recited in claim 23, the coprocessor further features a master cell (FIG. 2 – 126; page 10, lines 16-20) for forwarding array programs to the processing cells of the two-dimensional array.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on Appeal are: (1) the rejection of claim 13 under 35 U.S.C. § 102 over Callahan et al. "*The Garp architecture and C compiler*" ("Callahan"); (2) the rejection of claims 1, 4, 6-8, 12 and 20-23 under 35 U.S.C. § 103 over Callahan in view of Page "Reconfigurable Processors" ("Page");

(3) the rejections of claims 2, 3, 5, and 15 under 35 U.S.C. § 103 over Callahan in view of Page and further in view of Miyamori et al. "REMARC: Reconfigurable multimedia array coprocessor" ("Miyamori"); (4) the rejection of claim 11 under 35 U.S.C. § 103 over Callahan in view of Page and further in view of Taylor U.S. Patent 5,857,109 ("Taylor"); and (5) the rejection of claims 14 and 16-18 under 35 U.S.C. § 103 over Callahan in view of Barat et al. "*Reconfigurable instruction set processor: An implementation platform for interactive multimedia applications*" ("Barat").

ARGUMENTS

(1) Claim 13 Is Patentable Over Callahan

Among other things, the unit of claim 13 includes a mechanism for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array.

Applicants respectfully submit that Callahan does not disclose a function unit including such a mechanism.

The Examiner cites Figure 1 and page 63, column 1, paragraph 9 of Callahan as supposedly disclosing such a feature as the "programmable wiring."

Applicants respectfully disagree.

Claim 13 recites that the mechanism reconfigures a plurality of intra-processor information paths to the array.

In contrast, page 63, column 1, paragraph 9 of Callahan discloses that "the Garp array is a two-dimensional ***array of CLBs interconnected by programmable wiring***." Thus, the cited text in Callahan merely discloses that the interconnections between the CLBs ***within*** the gate array are programmable, but it certainly does not disclose that the programmable wiring "reconfigures a plurality of ***intra***-processor information paths to the array." So Callahan merely discloses a conventional field programmable gate array (FPGA).

Accordingly, for at least these reasons, Applicants respectfully submit that claim 13 is patentable over Callahan.

(2) Claims 1, 4, 6-8, 12 and 20-23 Are Patentable over Callahan in view of Page

Claim 1

Among other things, the coprocessor of claim 1 is connected to the processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

The Examiner states that Callahan discloses such a combination of features.

Applicants respectfully disagree

As explained above with respect to claim 13, Callahan merely discloses that the interconnections between the CLBs ***within*** the gate array are programmable, but it certainly does not disclose that the programmable wiring "reconfigures a plurality of ***intra***-processor information paths to the array."

The Examiner does not allege that Page discloses such a feature, and of course it does not. So no combination of Callahan and Page could ever produce the coprocessor of claim 1.

Furthermore, Applicants respectfully traverse the proposed combination of Callahan and Page with respect to claim 1 as lacking any reason in the prior art for the proposed combination. The text on page 1, paragraph 2 of Page that supposedly provides a reason to modify Callahan has nothing at all to do with the proposed modification of Callahan. More specifically, nothing in the cited text indicates at all that modifying Callahan such that the coprocessor has an execution speed greater than that of the processor would "*effectively target the processor in a wide array of applications*."

Accordingly, for at least these reasons, Applicants respectfully submit that claim 1 is patentable over the cited art.

Claims 4, 6-8 and 12

Claims 4, 6-8 and 12 all depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1.

Claim 20

Among other things, the method of claim 20 includes communicatively connecting the coprocessor to the processor by an interface module having a

mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

The Examiner states that Callahan discloses such a combination of features.

Applicants respectfully disagree

As explained above with respect to claims 13 and 1, Callahan merely discloses that the interconnections between the CLBs ***within*** the gate array are programmable, but it certainly does not disclose that the programmable wiring reconfigures ***a plurality of information paths BETWEEN the interface module and respective cells on a periphery of the array***.

The Examiner does not allege that Page discloses such a feature, and of course it does not. So no combination of Callahan and Page could ever produce the method of claim 20.

Furthermore, Applicants respectfully traverse the proposed combination of Callahan and Page with respect to claim 20 as lacking any reason in the prior art, for reasons set forth above with respect to claim 1.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 20 is patentable over the cited art.

Claim 21

In the coprocessor of claim 21, the array is rectangular, wherein the periphery consists of those of the processing cells located in all of a first row, last row, first column and last column of the array, and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array.

None of the cited references, alone or in combination, disclose or suggest a mechanism reconfigures information paths ***directly connecting the interface module and each of the cells on the periphery of the array***.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 21 is patentable over the cited art.

Claim 22

In the coprocessor of claim 22, the interface comprises a plurality of ***border cells directly connected to the respective processing cells on the periphery of the array***.

None of the cited references, alone or in combination, disclose or suggest an interface that comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array.

The Examiner cites Callahan's control blocks as supposedly corresponding to the recited plurality of border cells.

However, Callahan clearly discloses at the bottom of the first column of page 64 that "*control blocks reside in the array's leftmost column, one per row.*" That is, the control block are the ***processing cells on the periphery of the array*** and therefore cannot also be border cells directly connected to the respective processing cells on the periphery of the array.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 22 is patentable over the cited art.

Claim 23

The coprocessor of claim 23 includes a master cell for forwarding array programs to the processing cells of the two-dimensional array.

None of the cited references, alone or in combination, disclose or suggest a coprocessor that includes such a master cell.

In claim 22, the Examiner argues that Callahan's control block corresponded to Applicants' recited border cells. Now, in claim 23, the Examiner argues that Callahan's control block corresponded to Applicants' recited master cell.

Of course, Callahan's control block does not correspond to either, because Callahan's control blocks do not forward array programs to the processing cells of the two-dimensional array. Callahan clearly teaches that the control blocks provide a ***control interface*** (as opposed to a data interface) to the memory or processor (e.g., initiating a memory access; acting as a loop exit; etc.) (see bottom of first column on page 64). But Callahan does not teach that the control blocks forward array programs to the processing cells.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 230 is patentable over the cited art.

(3) Claims 2, 3, 5, and 15 Are Patentable over Callahan, Page and Miyamori

Claims 2, 3 and 5 depend from claim 1, and claim 15 depends from claim 13. Applicants respectfully submit that Miyamori does not remedy the shortcomings of Callahan as set forth above with respect to claim 13, and Callahan and Page as set forth above with respect to claim 1. Therefore, Applicants respectfully submits that claims 2, 3, 5 and 15 are patentable for at least the reasons set forth above with respect to claims 1 and 13, respectively, and for at least the following additional reasons.

Applicants respectfully traverse the proposed combination of Callahan and Page with Miyamori as lacking any reason in the prior art. The text on page 389, column 2, paragraph 3 of Miyamori that supposedly provides the reason to modify Callahan has nothing to do with the proposed modifications. Tellingly, the exact same text and exact same supposed "motivation" are provided for modifying Callahan to include each of the various and diverse features cited in claims 2, 3 and 5. Clearly, this makes no sense, as the same supposed benefit cannot reasonably be argued to be provided separately by each of the various features of claims 2, 3 and 5!

Furthermore, with respect to claims 5 and 15, Applicants respectfully submit that the proposed modification of Callahan is contrary to M.P.E.P. § 2143.01 (V) and M.P.E.P. § 2143.01 (VI) as the entire point of Callahan is to provide total flexibility in the configuration of interconnections within the array, and this would be destroyed if inter-cell connections within the array were limited such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

Accordingly, for at least these additional reasons, Applicants respectfully submits that claims 2, 3, 5 and 15 are patentable over the cited art.

(4) Claim 11 is Patentable over Callahan, Page and Taylor

Claim 11 depends from claim 1. Applicants respectfully submit that Taylor does not remedy the shortcomings of Callahan and Page as set forth above with respect to claim 1. Therefore, Applicants respectfully submits that claim 11 is patentable for at least the reasons set forth above with respect to claim 1.

(5) Claims 14 and 16-18 Are Patentable over Callahan in view of Barat

Claims 14 and 16-18 depend from claim 13. Applicants respectfully submit that Barat does not remedy the shortcomings of Callahan as set forth above with respect to claim 13. Therefore, Applicants respectfully submits that claims 14 and 16-18 are patentable for at least the reasons set forth above with respect to claim 13, and for at least the following additional reasons.

With respect to claim 17, the system includes an array program generator for generating array programs to be transmitted, and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to the mechanism to correspondingly update a current steady state connection pattern of the intra-processor information paths.

Applicants respectfully submit that Barat does not disclose transmitting a reconfigure signal to the mechanism to correspondingly update a current steady state connection pattern of the intra-processor information paths, and specifically does not disclose such a feature in page 483, columns 1, paragraph 3.

Accordingly, for at least this additional reason, Applicants respectfully submit that claim 17 is patentable over the cited art.

CONCLUSION

For all of the foregoing reasons, Applicants submit that claims 1-7 and 9-14 are all patentable over the cited prior art. Therefore, Applicants respectfully request that the rejections of claims 1-7 and 9-14 be withdrawn, the claims be allowed, and the application be passed to issue.

If necessary, the Commissioner is hereby authorized in this reply to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any

additional fees required under 37 C.F.R. § 1.16, 37 C.F.R. § 1.17 or 37 C.F.R. § 41.20, particularly extension of time fees or any additional fee required for filing this Appeal Brief.

Respectfully submitted,

VOLENTINE & WHITT

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CLAIMS APPENDIX

1. (Previously Presented) A coprocessor to a main processor having an execution speed greater than that of said processor, the coprocessor comprising a two-dimensional array of processing cells and being communicatively connected to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

2. (Previously Presented) The coprocessor of claim 1, wherein the array comprises a systolic processing array.

3. (Previously Presented) The coprocessor of claim 1, wherein the paths are connected one-to-one with said respective cells.

4. (Previously Presented) The coprocessor of claim 1, wherein the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths.

5. (Previously Presented) The coprocessor of claim 1, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

6. (Previously Presented) A coprocessing system including the coprocessor, interface module and main processor of claim 1 and a shared memory that communicatively connects with the interface module and the main processor to provide the main processor to coprocessor connection.

7. (Previously Presented) The coprocessor of claim 1, including an array processor that comprises said two-dimensional array.

8. (Previously Presented) An integrated circuit comprising the coprocessor of claim 1.

9-10. (Canceled)

11. (Previously Presented) The coprocessor of claim 1, wherein said processor comprises a digital signal processor.

12. (Previously Presented) The coprocessor of claim 1, wherein said processor comprises a general purpose processor.

13. (Previously Presented) A functional unit having two-dimensional array of processing cells and serving as a component of a main processor, the unit having a mechanism for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array.

14. (Previously Presented) The unit of claim 13, wherein said processor comprises a very long instruction word (VLIW) processor.

15. (Previously Presented) The unit of claim 13, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

16. (Previously Presented) The unit of claim 13, further including means for transmitting a plurality of array programs to corresponding predetermined subsets of said processing cells.

17. (Previously Presented) A system including the processor of claim 16, and an array program generator for generating array programs to be transmitted, and,

when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths.

18. (Previously Presented) The system of claim 17, further including a compiler configured for receiving, in response to said program updating, data representative of input and output timing for said unit and further configured for compiling an instruction based on said data.

19. (Canceled)

20. (Previously Presented) A method for interfacing a coprocessor to a main processor, comprising the steps of:

configuring the coprocessor to compromise a two-dimensional array of processing cells and to have an execution speed greater than that of said processor; and

communicatively connecting the coprocessor to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

21. (Previously Presented) The coprocessor of claim 1, wherein the array is rectangular, wherein the periphery consists of those of said processing cells located in all of a first row, last row, first column and last column of said array, and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array.

22. (Previously Presented) The coprocessor of claim 1, wherein the interface comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array.

23. (Previously Presented) The coprocessor of claim 1, further comprising a master cell for forwarding array programs to the processing cells of the two-dimensional array.

EVIDENCE APPENDIX

{None}

RELATED PROCEEEDINGS APPENDIX

{None}